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[Title of Invention] SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

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[Proof] required

[Document Name] Specification

[Title of the Invention] Semiconductor Device And Manufacturing Thereof

[Scope of Claims]

[Claim 1]

A semiconductor device including a CMOS circuit formed by an n-channel TFT and a p-channel TFT, characterized in that:

the CMOS circuit has a structure that an active layer is sandwiched by a first wiring line and a second wiring line through an insulating layer in only the n-channel TFT,

the active layer includes a low concentration impurity region that is in contact with the channel formation region; and

the low concentration impurity region is formed to overlap the first wiring line and not to overlap the second wiring line.

[Claim 2]

A semiconductor device according to claim 1, characterized in that the first wiring line is electrically connected with the second wiring line.

[Claim 3]

A semiconductor device including a CMOS circuit formed by an n-channel TFT and a p-channel TFT, characterized in that:

the CMOS circuit has a structure that an active layer is sandwiched by a first wiring line and a second wiring line through an insulating layer in only the n-channel TFT; and

the second wiring line has a portion of a laminated

structure of a first conductive layer and a second conductive layer, and a portion of a structure in which a third conductive layer is wrapped by the first conductive layer and the second conductive layer.

[Claim 4]

A semiconductor device according to claim 3, characterized in that the third conductive layer has a lower resistance value than a first conductive layer or the second conductive layer.

[Claim 5]

A semiconductor device according to claim 3, characterized in that the first wiring line or the second wiring line is a conductive film mainly containing an element selected from the group consisting of tantalum (Ta), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si), or an alloy film or silicide film containing the above elements in combination.

[Claim 6]

A semiconductor device according to claim 3, characterized in that the third wiring line is a conductive film mainly containing aluminum (Al) or copper (Cu).

[Claim 7]

A semiconductor device including a pixel matrix circuit that has a pixel TFT formed by an n-channel TFT and a storage capacitor, characterized in that:

the pixel TFT has a structure that an active layer is sandwiched by a first wiring line and a second wiring line

through an insulating layer,

the active layer includes a low concentration impurity region that is in contact with the channel formation region; and

the low concentration impurity region is formed to overlap the first wiring line and not to overlap the second wiring line.

[Claim 8]

A semiconductor device according to claim 7, characterized in that the first wiring line is kept at the ground electric potential or at the source power supply electric potential.

[Claim 9]

A semiconductor device according to claim 7, characterized in that the first wiring line is kept at the floating electric potential.

[Claim 10]

A semiconductor device including a pixel matrix circuit that has a pixel TFT formed by an n-channel TFT and a storage capacitor, characterized in that:

the pixel TFT has a structure that an active layer is sandwiched by a first wiring line and a second wiring line through an insulating layer,

the second wiring line has a portion of a laminated structure of a first conductive layer and a second conductive layer, and a portion of a structure in which a third conductive layer is wrapped by the first conductive layer and the second

conductive layer.

[Claim 11]

A semiconductor device according to claim 10, characterized in that the third conductive layer has a lower resistance value than the first conductive layer or the second conductive layer.

[Claim 12]

A semiconductor device according to claim 10, characterized in that the first wiring line or the second wiring line is a conductive film mainly containing an element selected from the group consisting of tantalum (Ta), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si), or an alloy film or silicide film containing the above elements in combination.

[Claim 13]

A semiconductor device according to claim 10, characterized in that the third wiring line is a conductive film mainly containing aluminum (Al) or copper (Cu).

[Claim 14]

A semiconductor device having a pixel matrix circuit and a driver circuit that are formed on the same substrate, characterized in that:

a pixel TFT included in the pixel matrix circuit and an n-channel TFT included in the driver circuit have a structure that an active layer is sandwiched by a first wiring line and a second wiring line through an insulating layer; and

the first wiring line connected to the pixel TFT is

kept at the fixed electric potential or the floating electric potential, and the first wiring connected to the n-channel TFT included in the driver circuit is kept at the same level of electric potential as the second wiring line connected to the n-channel TFT included in the said driver circuit.

[Claim 15]

A semiconductor device according to claim 14, characterized in that the active layer includes a low concentration impurity region that is in contact with the channel formation region; and

the low concentration impurity region is formed to overlap the first wiring line and not to overlap the second wiring line.

[Claim 16]

A semiconductor device according to claim 14, characterized in that the second wiring line has a portion of a laminated structure of a first conductive layer and a second conductive layer, and a portion of a structure in which a third conductive layer is wrapped by the first conductive layer and the second conductive layer.

[Claim 17]

A semiconductor device according to claim 14, characterized in that the third conductive layer has a lower resistance value than a first conductive layer or the second conductive layer.

[Claim 18]

A semiconductor device according to claim 14,

characterized in that the first wiring line or the second wiring line is a conductive film mainly containing an element selected from the group consisting of tantalum (Ta), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si), or an alloy film or silicide film containing the above elements in combination.

[Claim 19]

A semiconductor device according to claim 14, characterized in that the third wiring line is a conductive film mainly containing aluminum (Al) or copper (Cu).

[Claim 20]

A semiconductor device, characterized in that the semiconductor device according to any one of claims 1 to 19 is an active matrix liquid crystal display or an active matrix EL display.

[Claim 21]

A semiconductor device, characterized in that the semiconductor device according to any one of claims 1 to 19 is a video camera, a digital camera, a projector, a projection TV, a goggle type display, an automobile navigation system, a personal computer, or a portable information terminal.

[Claim 22]

A manufacturing method of a semiconductor device including a CMOS circuit formed by an n-channel TFT and a p-channel TFT comprising:

a process of forming a first wiring line on a substrate,

a process of forming a first insulating layer on the

first wiring line,

a process of forming active layers, an active layer of the n-channel TFT and an active layer of the p-channel TFT, on the first insulating layer,

a process of forming a second insulating layer to overlap the active layer of the n-channel TFT and the active layer of the p-channel layer, and

a process of forming a second wiring line on the second insulating layer; and

characterized in that the first wiring line is formed to cross only the active layer of the n-channel TFT.

[Claim 23]

A manufacturing method of a semiconductor device according to claim 22, characterized in that the second wiring line has a portion of a laminated structure of a first conductive layer and a second conductive layer, and a portion of a structure in which a third conductive layer is wrapped by the first conductive layer and the second conductive layer.

[Claim 24]

A manufacturing method of a semiconductor device including a CMOS circuit formed by an n-channel TFT and a p-channel TFT comprising:

a process of forming a first wiring line on a substrate,

a process of forming a first insulating layer on the first wiring line,

a process of forming active layers, an active layer of the n-channel TFT and an active layer of the p-channel TFT,

on the first insulating layer,

a process of forming a second insulating layer to overlap the active layer of the n-channel TFT and the active layer of the p-channel layer,

a process of forming a first conductive layer on the second insulating layer,

a process of forming a patterned third conductive layer on the first conductive layer, and

a process of forming a second conductive layer to overlap the third conductive layer; and

characterized in that the first wiring line is formed to cross only the active layer of the n-channel TFT.

[Claim 25]

A manufacturing method of a semiconductor device according to claim 23 or 24, characterized in that a material with a lower resistance value than the first conductive layer or the second conductive layer is used as the third conductive layer.

[Claim 26]

A manufacturing method of a semiconductor device according to claim 23 or 24, characterized in that the first wiring line or the second wiring line is a conductive film mainly containing an element selected from the group consisting of tantalum (Ta), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si), or an alloy film or silicide film containing the above elements in combination.

[Claim 27]